

**WHAT IS CLAIMED IS:**

1           1.       A current mirror, comprising:  
2           a first leg comprising a reference current source operable to generate a  
3           reference current;  
4           a first mirror current leg comprising a first P-type CMOS transistor and a first  
5           N-type transistor;  
6           a second mirror current leg comprising a second P-Type CMOS transistor and  
7           a second N-type transistor;  
8           a load leg comprising a third P-type transistor and a load; and  
9           compensation circuitry operable to compensate for gate current leakage in said  
10          first, second and third P-type CMOS transistors.

1           2.       The current source according to claim 1, wherein said reference current  
2           is passed through an N-type CMOS transistor connected in a diode configuration.

1           3.       The current mirror according to claim 1, wherein said compensation  
2           circuitry comprises first and second P-type compensation transistors.

1           4.       The current mirror according to claim 3, wherein said first  
2           compensation transistor is connected in a diode configuration and is operable to sense  
3           and provide the portion of the copied reference current that is lost due to gate current  
4           leakage of said first, second and third P-type CMOS transistors.

1           5.       The current mirror according to claim 4, wherein said second P-type  
2   compensation transistor generates a compensation current equal to the portion of the  
3   copied reference current that is lost due to the gate current leakage of said first,  
4   second and third P-type CMOS transistors.

1           6.       The current mirror according to claim 5, wherein said load comprises a  
2   charge pump circuit for a phase-locked loop.

1           7.       The current mirror according to claim 5, wherein said current mirror  
2   comprises at least three output current sources.

1           8.       The current mirror according claim 7, wherein current mirror  
2   comprises a first sensing transistor in a diode configuration and at least three  
3   compensation devices to compensate for gate current leakage in said first, second and  
4   third P-type CMOS transistors.

1           9.       The current mirror according to claim 8, wherein said compensation  
2   devices comprise P-type CMOS transistors.

1           10.      The current mirror according to claim 9, wherein said three output  
2   current sources each comprise at least one P-type CMOS transistor and wherein said  
3   compensation devices compensate for gate current leakage in said P-type CMOS  
4   transistors.

1           11.     A method of operating a current mirror having a reference leg, first and  
2     second mirror legs each comprising at least one P-type CMOS transistor and a load  
3     leg, comprising:  
4           generating a known reference current in said reference leg of said current  
5           mirror circuit;  
6           using said reference current to control the flow of current in said first and  
7           second mirror legs and said load leg of said current mirror circuit;  
8           compensating for gate current leakage in said P-type CMOS transistors in said  
9           first and second mirror legs and the output load leg, thereby generating  
10          a current flow in said load leg equal to the current flow in said  
11          reference leg.

1           12.     The method according to claim 11, wherein said reference current is  
2     passed through an N-type CMOS transistor connected in a diode configuration.

1           13.     The method according to claim 12, wherein said compensation  
2     circuitry comprises first and second P-type compensation transistors.

1           14.     The method according to claim 13, wherein said first compensation  
2     transistor senses and generates the compensation current equal to the sum of all net  
3     gate current leakage through the diode connection of the first P-type CMOS transistor  
4     in the first mirror leg of said all P-type CMOS transistors.

1           15.     The method according to claim 14, wherein said second P-type  
2     compensation transistor copies the compensation current from the first P-type  
3     compensation transistor and adds the compensation current to the mismatched output  
4     current.

1           16.     The method according to claim 15, wherein said load comprises a  
2     charge pump circuit for a phase-locked loop.

1           17.     The method according to claim 15, wherein said current mirror  
2     comprises at least three output load legs.

1           18.     The method according claim 17, wherein said current mirror comprises  
2     at least three compensation devices plus the very first sensing compensation device to  
3     compensate for gate current leakage in said all legs containing a P-type CMOS  
4     transistor.

1           19.     The method according to claim 18, wherein said compensation devices  
2     comprise P-type CMOS transistor.

1           20.     The method according to claim 19, wherein said three output current  
2     mirror legs each comprise at least one P-type CMOS transistor and said three current  
3     compensation devices each provide compensation for all of said P-type CMOS  
4     transistors.